ML501 Reference Design

User Guide

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XILINX®

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
06/18/07	1.0	Initial Xilinx release.

Table of Contents

About This Guide

This user guide introduces several designs that demonstrate the Virtex™-5 LX device features using the using the ML501 Evaluation Platform.

Additional Documentation

The following documents are also available for download at http://www.xilinx.com/virtex5.

- Virtex-5 Family Overview

  The features and product selection of the Virtex-5 family are outlined in this overview.

- Virtex-5 Data Sheet: DC and Switching Characteristics

  This data sheet contains the DC and Switching Characteristic specifications for the Virtex-5 family.

- XtremeDSP™ Design Considerations

  This guide describes the XtremeDSP slice and includes reference designs for using the DSP48E slice.

- Virtex-5 Configuration Guide

  This all-encompassing configuration guide includes chapters on configuration interfaces (serial and SelectMAP), bitstream encryption, Boundary-Scan and JTAG configuration, reconfiguration techniques, and readback through the SelectMAP and JTAG interfaces.

- Virtex-5 Packaging Specifications

  This specification includes the tables for device/package combinations and maximum I/Os, pin definitions, pinout tables, pinout diagrams, mechanical drawings, and thermal specifications.

Additional Support Resources

To search the database of silicon and software questions and answers, or to create a technical support case in WebCase, see the Xilinx website at: http://www.xilinx.com/support.

Typographical Conventions

This document uses the following typographical conventions. An example illustrates each convention.

Convention	Meaning or Use	Example
Italic font	References to other documents	See the Virtex-5 *Configuration Guide* for more information.
	Emphasis in text	The address (F) is asserted *after* clock event 2.
Underlined Text	Indicates a link to a web page.	http://www.xilinx.com/virtex5

Online Document

The following conventions are used in this document:

Convention	Meaning or Use	Example
Blue text	Cross-reference link to a location in the current document	See the section "Additional Documentation" for details.
Red text	Cross-reference link to a location in another document	See Figure 2-5 in the *Virtex-5 Data Sheet*
Blue, underlined text	Hyperlink to a website (URL)	Go to http://www.xilinx.com for the latest documentation.

ML501 Reference Design

Introduction

The Virtex-5 family of FPGAs [Ref 1] offers designers multiple platforms with an optimized balance of high-performance logic, serial connectivity, signal processing, and embedded processing resources. All members of the Virtex-5 family are built using the second generation Advanced Silicon Modular Block (ASMBL™) technology and a state-of-the-art 65 nm copper process to produce the industry's highest performance FPGAs.

Along with capabilities offered directly through an integrated IP block implemented in silicon, the Xilinx LogiCORE IP catalog and the embedded processing IP catalog are available to system level designers. Constructing embedded processing systems is significantly simplified by the Base System Builder (BSB) wizard provided as part of the Embedded Development Kit (EDK).

Users can obtain a quick understanding of the features offered by the ML501 boards by running the demonstration content provided on the CompactFlash (CF) card included with each board. *ML501 Getting Started Tutorial* [Ref 2] shows how to configure the ML501 from the ACE files pre-loaded on the CF card and describes what to observe for expected output.

Reference Designs

Base System Builder

The BSB wizard helps designers quickly create a working embedded system using a point-and-click GUI to select a Xilinx processor and an associated set of desired peripherals. BSB generated designs for the ML501 are available at:

- http://www.xilinx.com/products/boards/ml501/reference_designs.htm#bsb_design

The tutorial describes how to use the EDK BSB wizard, described in the *Embedded System Tools Reference Manual* [Ref 4], to create a hardware design for the ML501 platform. Figure 1 shows a block diagram of the MicroBlaze™ processor based embedded system generated by BSB. A set of basic software test applications are also generated to verify the functionality of the peripherals instantiated within the BSB design.

The BSB design can be further customized within the Xilinx Platform Studio (XPS) environment to add additional standard EDK IP or user-created IP cores.

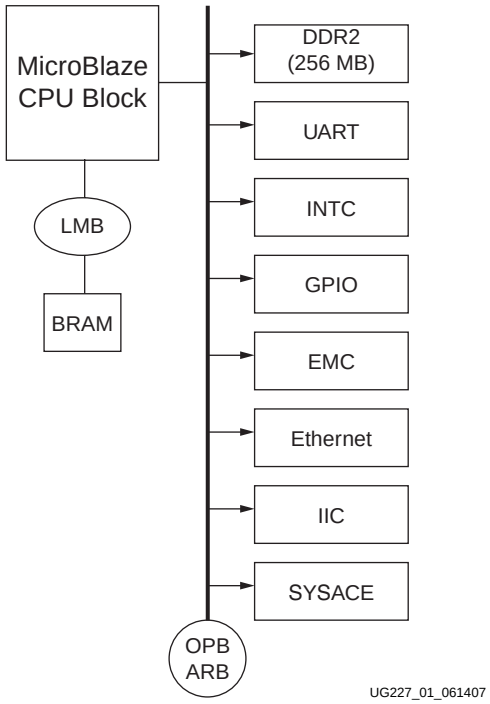

Figure 1: **Base System Builder Block Diagram**

EDK Design

This ML501 reference design utilizes the Embedded Development Kit (EDK) to create an embedded processing system using the MicroBlaze processor and the extensive set of peripherals offered through the EDK IP catalog. The ML501 EDK reference design contains a complete EDK project that can be used to explore the features of the ML501 platforms. The *Overview and Setup* presentation shows how to set up the design and the test environment. The *Stand-Alone Application* presentation shows how to exercise the reference design using the included software applications. EDK designs for the ML501 are available at:

- http://www.xilinx.com/products/boards/ml501/reference_designs.htm#ref_design

Figure 2 shows a high-level block diagram of the hardware used in the ML501 reference design.

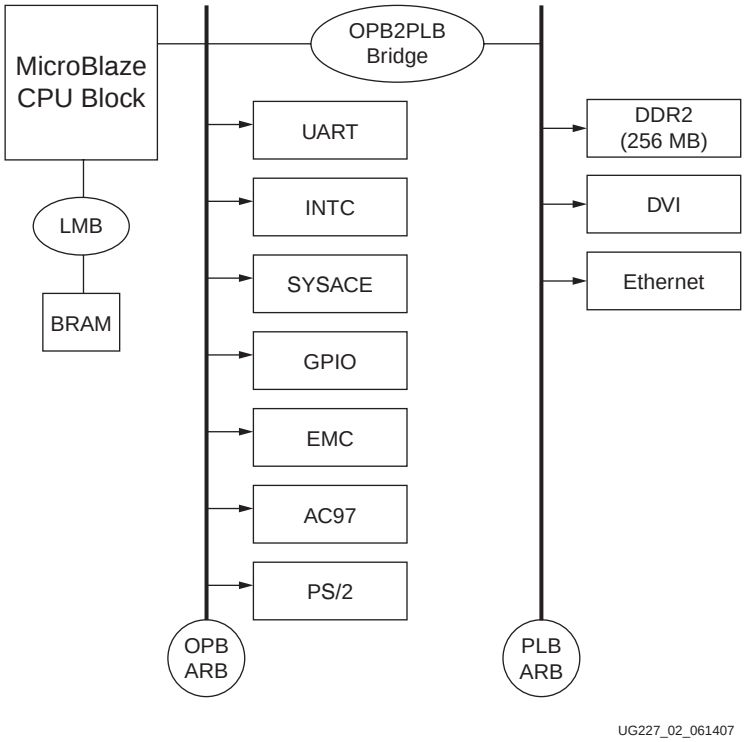

Figure 2: **ML501 High-Level Block Diagram**

Stand-Alone Software Applications

Software applications (Table 1) that run on the EDK hardware reference design can be compiled within EDK and downloaded to the ML501 with a JTAG download cable for verification. A set of pre-built ELF and ACE files as well as a `readme.txt` file explaining how to run each of the applications for the ML501 are available at:

- http://www.xilinx.com/products/boards/ml501/reference_designs.htm#ref_design

Table 1: **Demonstration Software Applications**

Name	Description
ml501_mb_standalone_apps_bit_elf_ace.zip	Complete collection of stand-alone BIT, ELF, and ACE files. To run each application individually, select one of the ACE files and replace `system_my_ace.ace` in configuration address 6 of the production ML501 CF card.
download.bit	MicroBlaze embedded processing system running bootloop code.
bootload.elf bootload.ace bootload_readme.txt	Main menu to load and launch ACE file demonstrations.
button_led_test.elf button_led_test.ace button_led_test_readme.txt	Verifies functionality of GPIO DIP switches, GPIO LEDs, N-E-S-W buttons and LEDs.
flash_hello.elf flash_hello_readme.txt	Placeholder application for a user-generated linear flash design. Loaded from linear flash.
flash_test.elf flash_test.ace flash_test_readme.txt	Tests linear flash memory.
hello.elf hello.ace hello_readme.txt	Exercises serial port output and input functionality using **`libc`** routines.
hello_uart.elf hello_uart.ace hello_uart_readme.txt	Exercises serial port output and input functionality using low-level UART driver routines.
iic_eeprom.elf iic_eeprom.ace iic_eeprom_readme.txt	Software bit-banging tests of IIC EEPROM.
my_ace.elf my_ace.ace my_ace_readme.txt	Placeholder application for a user-generated ACE file. Loaded from CompactFlash card.
my_plat_flash.elf my_plat_flash_readme.txt	Placeholder application for a user-generated Platform Flash design. Loaded from Platform Flash.
piezo.elf piezo.ace ringtones.zip piezo_readme.txt	Demonstrates audio output to the onboard piezo speaker using the ringtone RTTTL files.

Table 1: **Demonstration Software Applications *(Continued)***

Name	Description
ps2_scancodes_polled.elf ps2_scancodes_polled.ace ps2_scancodes_polled_readme.txt	Shows the scancodes from devices attached to the PS/2 input ports.
simon.elf simon.ace simon_readme.txt	Interactive game using N, E, S, W buttons and LEDs as well as the LCD panel.
slideshow.elf slideshow.ace slides.zip slideshow_readme.txt	A self-running audio and video presentation highlighting features of the ML501 and Virtex-5 technology.
spi_hello.elf spi_hello_readme.txt	Placeholder application for a user-generated SPI Flash design. Loaded from SPI Flash.
sysace_rebooter.elf sysace_rebooter.ace sysace_rebooter_readme.txt	User-selectable loading of ACE files utilizing the System ACE CF controller.
test_ac97.elf test_ac97.ace test_ac97_readme.txt	Records and plays back audio using the AC97 controller.
testfatfs.elf testfatfs.ace testfatfs.zip testfatfs_readme.txt	Write and read test of the FAT file system on the CompactFlash card.
usb_hpi_test.elf usb_hpi_test.ace demo.bin usb_hpi_test_readme.txt	USB host interface test utilizing a USB keyboard.
usb_printer.elf usb_printer.ace printer.bin usb_printer_readme.txt	USB host interface test utilizing a USB printer.
webserver.elf webserver.ace webserver_readme.txt	Web browser based control of GPIO LEDs and display of GPIO DIP switch status over Ethernet.
xrom.elf xrom.ace xrom_readme.txt	Board tests/diagnostics.

References

Documents supporting Virtex-5 devices and the ML501 Evaluation Platform are:

1. DS100, *Virtex-5 Family Overview: LX, LXT, and SXT Platforms*.
2. UG228, *ML501 Getting Started Tutorial*.
3. UG226, *ML501 Evaluation Platform User Guide*.
4. UG111, *Embedded System Tools Reference Manual, EDK 9.1i*.
5. UG191, *Virtex-5 FPGA Configuration User Guide*.
6. UG029, *ChipScope Pro Software and Cores User Guide*.